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## FACSIMILE COVER SHEET

DATE: May 15, 2006

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TELEPHONE:

FROM: Stephen A. Terrile
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SUBJECT: U.S. Serial Number 10/056,224
Attorney Docket No. P2678
Customer No.: 33438

This transmittal consists of 6 pages, including this cover sheet.

MESSAGE:

Enclosed for filing in U.S. Serial Number 10/056,224, please find a Reply Brief (5 pages). Thank you.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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|---|---|---|---|
| Applicant(s): | Hari K. Ravichandran | | |
| Assignee: | Sun Microsystems, Inc. | | |
| Title: | Apparatus and Method for Processor Performance Monitoring | | |
| Serial No.: | 10/056,244 | Filing Date: | January 22, 2002 |
| Examiner: | Aaron D. Matthew | Group Art Unit: | 2114 |
| Docket No.: | P2678 | Customer No.: | 33438 |

Austin, Texas
May 15, 2006

Mail Stop Appeal Brief - Patents
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United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

## REPLY BRIEF UNDER 37 CFR § 1.193

Dear Sir:

Applicants submit this Reply Brief pursuant to the Examiner's Answer mailed in this case on March 2, 2004. It is believed that no fees are due in connection with the filing of this Reply Brief, however, the Commissioner is authorized to deduct any amounts required for this Reply Brief and to credit any amounts overpaid to Deposit Account. No. 502264.

In response to Applicants arguments, the Examiner sets forth:

> Regarding the arguments supplied in the appeal brief for claim 9: (See pages 3-5 of the brief). The applicant argues that the prior art combination of Bunnell and Roeber does not individually or jointly teach or suggest 'method for monitoring an execution of a program which includes when the entry in the first memory device does not exist, generating at least one probe signal indicating a miss entry in the first memory device; generating a temporal identifier signal that is **associated with the probe signals**; and **storing the temporal identifier signal and the probe signals in memory**' (bottom of page 4, top of page 5 of the brief; emphasis added by the applicant). The examiner respectfully disagrees. The examiner contends that the prior art of record, Bunnell and Roeber, do teach the claimed invention. Bunnell discloses a 'miss cache signal' (lines 58-61 of Column 6), which the examiner equates to the claimed 'one probe signal indicating a miss entry in the first memory device,' as recited in the third limitation of

claim 9. The examiner further contends that Bunnell disclose a clock signal that is generated by the system clock the measures a time interval associated with the miss cache signal initiation. (lines 62-67 of Column 6 and Lines 1-5 of Column 7). The examiner equates this clock signal as the "temporal identifier that is associated with the probe signals" (limitation 4 of claim 9). Finally, the examiner contends that Bunnell also discloses a time register that stores the timer for the time interval of the miss cache signal. (Lines 39-60 of Column 7). The examiner acknowledges that the previous paragraphs have not been presented before in any action however, the examiner reminds applicant of the responsibility to read and consider the entirety of the reference for all that it discloses (Examiner's Answer, No. 10, Pages 17-18).

Applicants will address two points within the cited portion of the Examiner's Answer. The cache miss signal referenced by the examiner is generated by the cache memory itself (See Bunnell, Col. 6, lines 58 – 61) and thus is not generated as a result of searching a first memory device for an entry associated with a first address. The use of the term "probe signal" in claim 9 is intended to convey that the signal is generated external of the cache itself (see application, Page 4, lines 6 – 11) as compared with a miss signal (see application , page 7, lines 1 – 9). Additionally, because neither Bunnell nor Roeber disclose or suggest a "probe signal" as claimed, these reference could also not disclose or suggest a "temporal identifier signal" that is associated with the probe signal.

In response to Applicants arguments, the Examiner sets forth:

Regarding the arguments supplied in the appeal brief for claim 13: (See pages 3-5 of the brief). The applicant argues that the prior art combination of Bunnell and Roeber does not individually or jointly teach or suggest 'generating a second high-speed memory miss signal, a second high-speed memory miss count signal and a time stamp signal, the second high-speed memory miss signal indicating a miss in a second high-speed memory, the second high-speed memory miss count signal representing a number of misses in the second high-speed memory, and the time stamp signal indicating when the second high-speed memory miss signal is active.' (page 6 of the brief; emphasis added by the applicant). The applicant goes on to argue, 'it does not follow that it would have been obvious to analyze cache miss activity for multilevel or multiple caches as claimed merely because Levine discloses two levels of cache memory. The examiner respectfully disagrees. First, Bunnell disclose a need to check a second level of memory upon receiving a cache miss signal for a first memory. (Lines 55-58 of Column 6). Levine answers that need and includes checking of a second level of 'staging area memory' (the examiner reads this as a form of cache memory), before going to main system memory. Thereby, one of ordinary skill in the art would concluded that a first miss signal would be needed to check the first cache memory, and then a second missed cache signal would be need for the second memory, before attempting main system memory. Levine even goes so far as to say 'An access in which the required datum is missing from the cache is

called 'cache miss.' The ratio of cache misses to cache access is called the 'cache miss ratio.' Accompanying the cache miss ratio is the amount of time required to obtain the missing datum. The hierarchical cache levels are accessed sequentially. The first caches are usually the fastest but also the least capacious. Each subsequent cache is larger in capacity but slower to access." (Lines 8-15 of Column 2). Thereby, in the examiners opinion, Levine discloses a system that has multiple cache levels which require multiple cache miss signals that equates to the claimed second memory device with a probe signal. Levine also discloses the need to maintain quick access in higher level of hierarchical cache levels so as to maintain a faster rate of memory return. (Lines 12-15 of Column 2). The examiner equates this hierarchical cache levels as high-speed first and second memory levels. Therefore, Levine, in combination with Bunnell and Roeber provide "generating a second high-speed memory miss signal, a second high speed memory miss count signal and a time stamp signal, the second high-speed memory miss signal indicating a miss in a second high-speed memory, the second high-speed memory miss count signal representing a number of misses in the second high-speed memory, and the time stamp signal indication when the second high-speed memory miss signal is active," as stated in the claim 13. Thereby, Bunnell, Levine and Roeber taken together, in the examiner opinion, disclose all of the claimed invention (Examiner's Answer, No. 10, Pages 19-21).

Applicants will address a number of points within the cited portion of the Examiner's Answer. As discussed above, the cache miss signal referenced by the examiner is generated by the cache memory itself (See Bunnell, Col. 6, lines 58 – 61) and thus is not generated as a result of searching a first memory device for an entry associated with a first address. The use of the term "probe signal" in claim 9 is intended to convey that the signal is generated external of the cache itself (see application, Page 4, lines 6 – 11) as compared with a miss signal (see application , page 7, lines 1 – 9). Additionally, because neither Bunnell nor Roeber disclose or suggest a "probe signal" as claimed, these reference could also not disclose or suggest a "temporal identifier signal" that is associated with the probe signal.

Additionally, Applicant's respectfully disagree that merely disclosing multiple levels of cache discloses or suggests generating a second high – speed memory miss signal, a second high-speed memory miss count signal and a time stamp signal indicating when the second high-speed memory miss signal is active as claimed.

In response to Applicants arguments, the Examiner sets forth:

Regarding the arguments supplied in the appeal brief for claim 11: (See pages 6 of the brief). The applicant argues that the prior art combination of Bunnell, Roeber, and Levine does not individually or jointly teach or suggest 'a second memory device for an

entry associated with the first address, when the entry in the second memory device does not exist **generating at least one probe signal indicating a miss entry in the second memory device**, and generating a temporal identifier signal that is associated with the probe signal.' (page 6 of the brief; emphasis added by the applicant). The applicant goes on to argue, 'it does not follow that it would have been obvious to analyze cache miss activity for multilevel or multiple caches as claimed merely because Levine discloses two levels of cache memory. The examiner respectfully disagrees. First, Bunnell disclose a need to check a second level of memory upon receiving a cache miss signal for a first memory. (Lines 55-58 of Column 6). Levine answers that need and includes checking of a second level of 'staging area memory' (the examiner reads this as a form of cache memory), before going to main system memory. Thereby, one of ordinary skill in the art would concluded that a first miss signal would be needed to check the first cache memory, and then a second missed cache signal would be need for the second memory, before attempting main system memory. Levine even goes so far as to say 'An access in which the required datum is missing from the cache is called 'cache miss.' The ratio of cache misses to cache access is called the 'cache miss ratio.' Accompanying the cache miss ratio is the amount of time required to obtain the missing datum. The hierarchical cache levels are accessed sequentially. The first caches are usually the fastest but also the least capacious. Each subsequent cache is larger in capacity but slower to access." (Lines 8-15 of Column 2). Thereby, in the examiners opinion, Levine discloses a system that has multiple cache levels which require multiple cache miss signals that equates to the claimed second memory device with a probe signal. Therefore, Levin [sic], in combination with Bunnell and Roeber provide "a second memory device for an entry associated with the first address, when the entry in the second memory device does not exist generating at least one probe signal indication a miss entry in the second memory device, and generating a temporal identifier signal that is associated with the probe signal," as stated in the claim 11. Thereby, Bunnell, Levine and Roeber taken together, in the examiner opinion, disclose all of the claimed limitation.

Applicants will address a number of points within the cited portion of the Examiner's Answer. As discussed above, the cache miss signal referenced by the examiner is generated by the cache memory itself (See Bunnell, Col. 6, lines 58 – 61) and thus is not generated as a result of searching a first memory device for an entry associated with a first address. The use of the term "probe signal" indicating a miss entry in the second memory device in claim 11 is intended to convey that the signal is generated external of the cache itself (see application, Page 4, lines 6 – 11) as compared with a miss signal (see application , page 7, lines 1 – 9). Additionally, because neither Bunnell nor Roeber disclose or suggest a "probe signal" as claimed, these reference could also not disclose or suggest a "temporal identifier signal" that is associated with the probe signal.

For the above reasons, Applicants respectfully submits that the Examiner's rejections of Claims 9 - 19 are unfounded and should be reversed.

I hereby certify that this correspondence is being transmitted via facsimile to the USPTO on May 15, 2006.

Attorney for Applicants — Date of Signature: 5/15/06

Respectfully submitted,

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